

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 *            Zvector E6 instruction tests for VRX encoded:
				5 *
				6 *            E609 VSTEBRH - VECTOR STORE BYTE REVERSED ELEMENT (16)
				7 *            E60A VSTEBRG - VECTOR STORE BYTE REVERSED ELEMENT (64)
				8 *            E60B VSTEBRF - VECTOR STORE BYTE REVERSED ELEMENT (32)
				9 *            E60E VSTBR    - VECTOR STORE BYTE REVERSED ELEMENTS
				10 *           E60F VSTER    - VECTOR STORE ELEMENTS REVERSED
				11 *
				12 *            James Wekel June 2024
				13 *****
				15 *****
				16 *
				17 *            basic instruction tests
				18 *
				19 *****
				20 *    This program tests proper functioning of the z/arch E6 VRX vector
				21 *    store instructions. Exceptions are not tested.
				22 *
				23 *    PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				24 *    obvious coding errors. None of the tests are thorough. They are
				25 *    NOT designed to test all aspects of any of the instructions.
				26 *
				27 *****
				28 *
				29 *            *Testcase VECTOR E6 VRX store instructions
				30 *            *
				31 *            *            Zvector E6 instruction tests for VRX encoded:
				32 *            *
				33 *            *            E609 VSTEBRH - VECTOR STORE BYTE REVERSED ELEMENT (16)
				34 *            *            E60A VSTEBRG - VECTOR STORE BYTE REVERSED ELEMENT (64)
				35 *            *            E60B VSTEBRF - VECTOR STORE BYTE REVERSED ELEMENT (32)
				36 *            *            E60E VSTBR    - VECTOR STORE BYTE REVERSED ELEMENTS
				37 *            *            E60F VSTER    - VECTOR STORE ELEMENTS REVERSED
				38 *            *
				39 *            *            # -----
				40 *            *            #    This tests only the basic function of the instruction.
				41 *            *            #    Exceptions are NOT tested.
				42 *            *            # -----
				43 *            *
				44 *    main size            2
				45 *    numcpu              1
				46 *    sysclear
				47 *    archlvl             z/Arch
				48 *
				49 *    loadcore            "\$ (testpath) /zvector-e6-02-stores.core" 0x0
				50 *
				51 *    diag8cmd            enable    # (needed for messages to Hercules console)
				52 *    runtest             2
				53 *    diag8cmd            disable   # (reset back to default)
				54 *
				55 *            *Done
				56 *

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
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57 \*\*\*\*\*

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				59 *****
				60 * FCHECK Macro - Is a Facility Bit set?
				61 *
				62 * If the facility bit is NOT set, an message is issued and
				63 * the test is skipped.
				64 *
				65 * Fcheck uses R0, R1 and R2
				66 *
				67 * eg. FCHECK 134, 'vector-packed-decimal'
				68 *****
				69 MACRO
				70 FCHECK &BITNO, &NOTSETMSG
				71 . * &BITNO : facility bit number to check
				72 . * &NOTSETMSG : 'facility name'
				73 LCLA &FBBYTE Facility bit in Byte
				74 LCLA &FBBIT Facility bit within Byte
				75
				76 LCLA &L(8)
				77 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				78
				79 &FBBYTE SETA &BITNO/8
				80 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				81 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				82
				83 B X&SYSNDX
				84 * Fcheck data area
				85 * skip messgae
				86 SKT&SYSNDX DC C' Skipping tests: '
				87 DC C&NOTSETMSG
				88 DC C' facility (bit &BITNO) is not installed.'
				89 SKL&SYSNDX EQU *-SKT&SYSNDX
				90 * facility bits
				91 DS FD gap
				92 FB&SYSNDX DS 4FD
				93 DS FD gap
				94 *
				95 X&SYSNDX EQU *
				96 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				97 STFLE FB&SYSNDX get facility bits
				98
				99 XGR R0, R0
				100 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				101 N R0, =F' &FBBIT' is bit set?
				102 BNZ XC&SYSNDX
				103 *
				104 * facility bit not set, issue message and exit
				105 *
				106 LA R0, SKL&SYSNDX message length
				107 LA R1, SKT&SYSNDX message address
				108 BAL R2, MSG
				109
				110 B EOJ
				111 XC&SYSNDX EQU *
				112 MEND



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				133	
				134	*****
				135	* The actual "ZVE6TST" program itself...
				136	*****
				137	*
				138	* Architecture Mode: z/Arch
				139	* Register Usage:
				140	*
				141	* R0 (work)
				142	* R1-4 (work)
				143	* R5 Testing control table - current test base
				144	* R6- R7 (work)
				145	* R8 First base register
				146	* R9 Second base register
				147	* R10 Third base register
				148	* R11 E6TEST call return
				149	* R12 E6TESTS register
				150	* R13 (work)
				151	* R14 Subroutine call
				152	* R15 Secondary Subroutine call or work
				153	*
				154	*****
00000200		00000200		156	USING BEGIN, R8 FIRST Base Register
00000200		00001200		157	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		158	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			160	BEGIN BALR R8, 0 Initalize FIRST base register
00000202	0680			161	BCTR R8, 0 Initalize FIRST base register
00000204	0680			162	BCTR R8, 0 Initalize FIRST base register
00000206	4190 8800		00000800	164	LA R9, 2048(, R8) Initalize SECOND base register
0000020A	4190 9800		00000800	165	LA R9, 2048(, R9) Initalize SECOND base register
				166	
0000020E	41A0 9800		00000800	167	LA R10, 2048(, R9) Initalize THIRD base register
00000212	41A0 A800		00000800	168	LA R10, 2048(, R10) Initalize THIRD base register
				169	
00000216	B600 82A4		000004A4	170	STCTL R0, R0, CTLR0 Store CR0 to enable AFP
0000021A	9604 82A5		000004A5	171	OI CTLR0+1, X' 04' Turn on AFP bit
0000021E	9602 82A5		000004A5	172	OI CTLR0+1, X' 02' Turn on Vector bit
00000222	B700 82A4		000004A4	173	LCTL R0, R0, CTLR0 Reload updated CR0
				174	
				175	*****
				176	* Is Vector-enhancements facility 2 installed (bit 148
				177	*****
				178	
				179	FCHECK 148, 'Vector-enhancements facility 2'
00000226	47F0 80B8		000002B8	180+	B X0001
				181+	* Fcheck data area
				182+	* skip messgae
0000022A	40404040 40404040			183+	SKT0001 DC C' Skipping tests: '
00000244	E58583A3 96996085			184+	DC C' Vector-enhancements facility 2'
00000262	40868183 899389A3			185+	DC C' facility (bit 148) is not installed. '
		0000005D 00000001		186+	SKL0001 EQU *- SKT0001
				187+	* facility bits
00000288	00000000 00000000			188+	DS FD gap





[illegible]







LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				343	*****
				344	*            Normal completion or Abnormal termination PSWs
				345	*****
00000478	00020001 80000000			347	E0JPSW    DC    0D' 0' , X' 0002000180000000' , AD(0)
00000488	B2B2 8278		00000478	349	E0J            LPSWE E0JPSW            Normal completion
00000490	00020001 80000000			351	FAILPSW    DC    0D' 0' , X' 0002000180000000' , AD(X' BAD' )
000004A0	B2B2 8290		00000490	353	FAILTEST LPSWE FAILPSW            Abnormal termination
				355	*****
				356	*            Working Storage
				357	*****
000004A4	00000000			359	CTLR0       DS    F            CRO
000004A8	00000000			360	DS    F
000004AC				362	LTORG ,            Literals pool
000004AC	00000008			363	=F' 8'
000004B0	000014D0			364	=A(E6TESTS)
000004B4	00000001			365	=F' 1'
000004B8	0000			366	=H' 0'
000004BA	005F			367	=AL2(L' MSGMSG)
				368	
				369	*            some constants
				370	
	00000400	00000001		371	K            EQU    1024            One KB
	00001000	00000001		372	PAGE        EQU    (4*K)            Size of one page
	00010000	00000001		373	K64         EQU    (64*K)            64 KB
	00100000	00000001		374	MB          EQU    (K*K)            1 MB
				375	
	AABBCCDD	00000001		376	REG2PATT EQU    X' AABBCCDD'            Polluted Register pattern
	000000DD	00000001		377	REG2LOW EQU            X' DD'            (last byte above)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				418 *****
				419 *            E6TEST DSECT
				420 *****
				422 E6TEST    DSECT ,
00000000	00000000			423 TSUB      DC    A(0)            pointer to test
00000004	0000			424 TNUM     DC    H' 00'            Test Number
00000006	00			425           DC    X' 00'
00000007	00			426 MB       DC    X' 00'            MB used
				427
00000008	40404040	40404040		428 OPNAME   DC    CL8' '            E6 name
00000010	00000000			429 RELEN    DC    A(0)            RESULT LENGTH
00000014	00000000			430 READDR   DC    A(0)
				431
				432 *           test routine will be here (from VRX macro)
				433 *
				434 *           followed by
				435 *           EXPECTED RESULT
000010D4		00000000	00001533	437 ZVE6TST   CSECT ,
				438           DS    0F
				440 *****
				441 *           Macros to help build test tables
				442 *****
				444 *
				445 *    macro to generate individual test
				446 *
				447            MACRO
				448            VRX    &INST, &MB
				449 . *                            &INST    - VRX instruction under test
				450 . *                            &MB       - mB field
				451
				452            GBLA   &TNUM
				453 &TNUM     SETA   &TNUM+1
				454
				455            DS    0FD
				456            USING *, R5            base for test data and test routine
				457
				458 T&TNUM    DC    A(X&TNUM)           address of test routine
				459            DC    H' &TNUM           test number
				460            DC    X' 00'
				461            DC    X' &MB'            MB
				462            DC    CL8' &INST'       instruction name
				463            DC    A(16)            result length
				464 REA&TNUM DC    A(RE&TNUM)       result address
				465 . *
				466 *
				467            DS    0F
				468 X&TNUM    &INST V1, V10OUTPUT, &MB    test instruction



LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				498 *****
				499 * E6 VRX tests
				500 *****
				501 PRINT DATA
				502
				503 * E609 VSTEBRH - VECTOR STORE BYTE REVERSED ELEMENT (16)
				504 * E60A VSTEBRG - VECTOR STORE BYTE REVERSED ELEMENT (64)
				505 * E60B VSTEBRF - VECTOR STORE BYTE REVERSED ELEMENT (32)
				506 * E60E VSTBR - VECTOR STORE BYTE REVERSED ELEMENTS
				507 * E60F VSTER - VECTOR STORE ELEMENTS REVERSED
				508
				509 * VRX instruction, m3
				510 * followed by 16 byte expected result
				511 *-----
				512 * VSTEBRH - VECTOR STORE BYTE REVERSED ELEMENT (16)
				513 *-----
				514 VRX VSTEBRH, 0
000010D8				515+ DS OFD
000010D8		000010D8		516+ USING *, R5 base for test data and test routine
000010D8	000010F0			517+T1 DC A(X1) address of test routine
000010DC	0001			518+ DC H' 1' test number
000010DE	00			519+ DC X' 00'
000010DF	00			520+ DC X' 0' MB
000010E0	E5E2E3C5 C2D9C840			521+ DC CL8' VSTEBRH' instruction name
000010E8	00000010			522+ DC A(16) result length
000010EC	000010F8			523+REA1 DC A(RE1) result address
				524+*
000010F0				525+ DS OF
000010F0	E610 8E84 0009	00001084		526+X1 VSTEBRH V1, V10UTPUT, 0 test instruction
000010F6	07FB			527+ BR R11 return
000010F8				528+RE1 DC OF xl 16 result
000010F8				529+ DROP R5
000010F8	0100FFFF FFFFFFFF			530 DC XL16' 0100FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001100	FFFFFFFF FFFFFFFF			
				531
				532 VRX VSTEBRH, 1
00001108				533+ DS OFD
00001108		00001108		534+ USING *, R5 base for test data and test routine
00001108	00001120			535+T2 DC A(X2) address of test routine
0000110C	0002			536+ DC H' 2' test number
0000110E	00			537+ DC X' 00'
0000110F	01			538+ DC X' 1' MB
00001110	E5E2E3C5 C2D9C840			539+ DC CL8' VSTEBRH' instruction name
00001118	00000010			540+ DC A(16) result length
0000111C	00001128			541+REA2 DC A(RE2) result address
				542+*
00001120				543+ DS OF
00001120	E610 8E84 1009	00001084		544+X2 VSTEBRH V1, V10UTPUT, 1 test instruction
00001126	07FB			545+ BR R11 return
00001128				546+RE2 DC OF xl 16 result
00001128				547+ DROP R5
00001128	0302FFFF FFFFFFFF			548 DC XL16' 0302FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001130	FFFFFFFF FFFFFFFF			
				549
				550 VRX VSTEBRH, 2
00001138				551+ DS OFD



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001138		00001138		552+	USING *,R5	base for test data and test routine
00001138	00001150			553+T3	DC A(X3)	address of test routine
0000113C	0003			554+	DC H' 3'	test number
0000113E	00			555+	DC X' 00'	
0000113F	02			556+	DC X' 2'	MB
00001140	E5E2E3C5 C2D9C840			557+	DC CL8' VSTEBRH'	instruction name
00001148	00000010			558+	DC A(16)	result length
0000114C	00001158			559+REA3	DC A(RE3)	result address
				560+*		
00001150				561+	DS 0F	
00001150	E610 8E84 2009		00001084	562+X3	VSTEBRH V1,V10UTPUT, 2	test instruction
00001156	07FB			563+	BR R11	return
00001158				564+RE3	DC 0F	xl 16 result
00001158				565+	DROP R5	
00001158	0504FFFF FFFFFFFF			566	DC XL16' 0504FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	
00001160	FFFFFFFF FFFFFFFF					
				567		
00001168		00001168		568	VRX VSTEBRH, 3	
00001168				569+	DS 0FD	
00001168	00001180			570+	USING *,R5	base for test data and test routine
0000116C	0004			571+T4	DC A(X4)	address of test routine
0000116E	00			572+	DC H' 4'	test number
0000116E	00			573+	DC X' 00'	
0000116F	03			574+	DC X' 3'	MB
00001170	E5E2E3C5 C2D9C840			575+	DC CL8' VSTEBRH'	instruction name
00001178	00000010			576+	DC A(16)	result length
0000117C	00001188			577+REA4	DC A(RE4)	result address
				578+*		
00001180				579+	DS 0F	
00001180	E610 8E84 3009		00001084	580+X4	VSTEBRH V1,V10UTPUT, 3	test instruction
00001186	07FB			581+	BR R11	return
00001188				582+RE4	DC 0F	xl 16 result
00001188				583+	DROP R5	
00001188	0706FFFF FFFFFFFF			584	DC XL16' 0706FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	
00001190	FFFFFFFF FFFFFFFF					
				585		
00001198		00001198		586	VRX VSTEBRH, 4	
00001198				587+	DS 0FD	
00001198	000011B0			588+	USING *,R5	base for test data and test routine
0000119C	0005			589+T5	DC A(X5)	address of test routine
0000119C	0005			590+	DC H' 5'	test number
0000119E	00			591+	DC X' 00'	
0000119F	04			592+	DC X' 4'	MB
000011A0	E5E2E3C5 C2D9C840			593+	DC CL8' VSTEBRH'	instruction name
000011A8	00000010			594+	DC A(16)	result length
000011AC	000011B8			595+REA5	DC A(RE5)	result address
				596+*		
000011B0				597+	DS 0F	
000011B0	E610 8E84 4009		00001084	598+X5	VSTEBRH V1,V10UTPUT, 4	test instruction
000011B6	07FB			599+	BR R11	return
000011B8				600+RE5	DC 0F	xl 16 result
000011B8				601+	DROP R5	
000011B8	0908FFFF FFFFFFFF			602	DC XL16' 0908FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	
000011C0	FFFFFFFF FFFFFFFF					
				603		
				604	VRX VSTEBRH, 5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000011C8				605+	DS	0FD
000011C8		000011C8		606+	USING	*, R5
000011C8	000011E0			607+T6	DC	A(X6)
000011CC	0006			608+	DC	H' 6'
000011CE	00			609+	DC	X' 00'
000011CF	05			610+	DC	X' 5'
000011D0	E5E2E3C5 C2D9C840			611+	DC	CL8' VSTEBRH'
000011D8	00000010			612+	DC	A(16)
000011DC	000011E8			613+REA6	DC	A(RE6)
				614+*		
000011E0				615+	DS	0F
000011E0	E610 8E84 5009		00001084	616+X6	VSTEBRH	V1, V10UTPUT, 5
000011E6	07FB			617+	BR	R11
000011E8				618+RE6	DC	0F
000011E8				619+	DROP	R5
000011E8	1110FFFF FFFFFFFF			620	DC	XL16' 1110FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
000011F0	FFFFFFFF FFFFFFFF					
				621		
000011F8				622	VRX	VSTEBRH, 6
000011F8		000011F8		623+	DS	0FD
000011F8	00001210			624+	USING	*, R5
000011FC	0007			625+T7	DC	A(X7)
000011FE	00			626+	DC	H' 7'
000011FF	06			627+	DC	X' 00'
00001200	E5E2E3C5 C2D9C840			628+	DC	X' 6'
00001208	00000010			629+	DC	CL8' VSTEBRH'
0000120C	00001218			630+	DC	A(16)
				631+REA7	DC	A(RE7)
				632+*		
00001210				633+	DS	0F
00001210	E610 8E84 6009		00001084	634+X7	VSTEBRH	V1, V10UTPUT, 6
00001216	07FB			635+	BR	R11
00001218				636+RE7	DC	0F
00001218				637+	DROP	R5
00001218	1312FFFF FFFFFFFF			638	DC	XL16' 1312FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001220	FFFFFFFF FFFFFFFF					
				639		
00001228				640	VRX	VSTEBRH, 7
00001228		00001228		641+	DS	0FD
00001228	00001240			642+	USING	*, R5
0000122C	0008			643+T8	DC	A(X8)
0000122E	00			644+	DC	H' 8'
0000122F	07			645+	DC	X' 00'
00001230	E5E2E3C5 C2D9C840			646+	DC	X' 7'
00001238	00000010			647+	DC	CL8' VSTEBRH'
0000123C	00001248			648+	DC	A(16)
				649+REA8	DC	A(RE8)
				650+*		
00001240				651+	DS	0F
00001240	E610 8E84 7009		00001084	652+X8	VSTEBRH	V1, V10UTPUT, 7
00001246	07FB			653+	BR	R11
00001248				654+RE8	DC	0F
00001248				655+	DROP	R5
00001248	1514FFFF FFFFFFFF			656	DC	XL16' 1514FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001250	FFFFFFFF FFFFFFFF					
				657		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				658 *	-----
				659 *	VSTEBRG - VECTOR STORE BYTE REVERSED ELEMENT (64)
				660 *	-----
				661	VRX VSTEBRG, 0
00001258				662+	DS OFD
00001258		00001258		663+	USING *, R5
00001258	00001270			664+T9	DC A(X9)
0000125C	0009			665+	DC H' 9'
0000125E	00			666+	DC X' 00'
0000125F	00			667+	DC X' 0'
00001260	E5E2E3C5 C2D9C740			668+	DC CL8' VSTEBRG'
00001268	00000010			669+	DC A(16)
0000126C	00001278			670+REA9	DC A(RE9)
				671+*	
00001270				672+	DS OF
00001270	E610 8E84 000A		00001084	673+X9	VSTEBRG V1, V10UTPUT, 0
00001276	07FB			674+	BR R11
00001278				675+RE9	DC OF
00001278				676+	DROP R5
00001278	07060504 03020100			677	DC XL16' 0706050403020100FFFFFFFFFFFFFFFF'
00001280	FFFFFFFF FFFFFFFF				
				678	
				679	VRX VSTEBRG, 1
00001288				680+	DS OFD
00001288		00001288		681+	USING *, R5
00001288	000012A0			682+T10	DC A(X10)
0000128C	000A			683+	DC H' 10'
0000128E	00			684+	DC X' 00'
0000128F	01			685+	DC X' 1'
00001290	E5E2E3C5 C2D9C740			686+	DC CL8' VSTEBRG'
00001298	00000010			687+	DC A(16)
0000129C	000012A8			688+REA10	DC A(RE10)
				689+*	
000012A0				690+	DS OF
000012A0	E610 8E84 100A		00001084	691+X10	VSTEBRG V1, V10UTPUT, 1
000012A6	07FB			692+	BR R11
000012A8				693+RE10	DC OF
000012A8				694+	DROP R5
000012A8	15141312 11100908			695	DC XL16' 1514131211100908FFFFFFFFFFFFFFFF'
000012B0	FFFFFFFF FFFFFFFF				
				696	
				697	
				698 *	-----
				699 *	VSTEBRF - VECTOR STORE BYTE REVERSED ELEMENT (32)
				700 *	-----
				701	VRX VSTEBRF, 0
000012B8				702+	DS OFD
000012B8		000012B8		703+	USING *, R5
000012B8	000012D0			704+T11	DC A(X11)
000012BC	000B			705+	DC H' 11'
000012BE	00			706+	DC X' 00'
000012BF	00			707+	DC X' 0'
000012C0	E5E2E3C5 C2D9C640			708+	DC CL8' VSTEBRF'
000012C8	00000010			709+	DC A(16)
000012CC	000012D8			710+REA11	DC A(RE11)
				711+*	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000012D0				712+	DS	0F
000012D0	E610 8E84 000B		00001084	713+X11	VSTEBRF	V1, V10UTPUT, 0 test instruction
000012D6	07FB			714+	BR	R11 return
000012D8				715+RE11	DC	0F xl 16 result
000012D8				716+	DROP	R5
000012D8	03020100 FFFFFFFF			717	DC	XL16' 03020100FFFFFFFFFFFFFFFFFFFFFFFF'
000012E0	FFFFFFFF FFFFFFFF					
				718		
				719	VRX	VSTEBRF, 1
000012E8				720+	DS	0FD
000012E8		000012E8		721+	USING	*, R5 base for test data and test routine
000012E8	00001300			722+T12	DC	A(X12) address of test routine
000012EC	000C			723+	DC	H' 12' test number
000012EE	00			724+	DC	X' 00'
000012EF	01			725+	DC	X' 1' MB
000012F0	E5E2E3C5 C2D9C640			726+	DC	CL8' VSTEBRF' instruction name
000012F8	00000010			727+	DC	A(16) result length
000012FC	00001308			728+REA12	DC	A(RE12) result address
				729+*		
00001300				730+	DS	0F
00001300	E610 8E84 100B		00001084	731+X12	VSTEBRF	V1, V10UTPUT, 1 test instruction
00001306	07FB			732+	BR	R11 return
00001308				733+RE12	DC	0F xl 16 result
00001308				734+	DROP	R5
00001308	07060504 FFFFFFFF			735	DC	XL16' 07060504FFFFFFFFFFFFFFFFFFFFFFFF'
00001310	FFFFFFFF FFFFFFFF					
				736		
				737	VRX	VSTEBRF, 2
00001318				738+	DS	0FD
00001318		00001318		739+	USING	*, R5 base for test data and test routine
00001318	00001330			740+T13	DC	A(X13) address of test routine
0000131C	000D			741+	DC	H' 13' test number
0000131E	00			742+	DC	X' 00'
0000131F	02			743+	DC	X' 2' MB
00001320	E5E2E3C5 C2D9C640			744+	DC	CL8' VSTEBRF' instruction name
00001328	00000010			745+	DC	A(16) result length
0000132C	00001338			746+REA13	DC	A(RE13) result address
				747+*		
00001330				748+	DS	0F
00001330	E610 8E84 200B		00001084	749+X13	VSTEBRF	V1, V10UTPUT, 2 test instruction
00001336	07FB			750+	BR	R11 return
00001338				751+RE13	DC	0F xl 16 result
00001338				752+	DROP	R5
00001338	11100908 FFFFFFFF			753	DC	XL16' 11100908FFFFFFFFFFFFFFFFFFFFFFFF'
00001340	FFFFFFFF FFFFFFFF					
				754		
				755	VRX	VSTEBRF, 3
00001348				756+	DS	0FD
00001348		00001348		757+	USING	*, R5 base for test data and test routine
00001348	00001360			758+T14	DC	A(X14) address of test routine
0000134C	000E			759+	DC	H' 14' test number
0000134E	00			760+	DC	X' 00'
0000134F	03			761+	DC	X' 3' MB
00001350	E5E2E3C5 C2D9C640			762+	DC	CL8' VSTEBRF' instruction name
00001358	00000010			763+	DC	A(16) result length
0000135C	00001368			764+REA14	DC	A(RE14) result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001360				765+*		
00001360	E610 8E84 300B		00001084	766+	DS OF	
00001366	07FB			767+X14	VSTBRF V1, V10UTPUT, 3	test instruction
00001368				768+	BR R11	return
00001368				769+RE14	DC OF	xl16 result
00001368				770+	DROP R5	
00001368	15141312 FFFFFFFF			771	DC XL16' 15141312FFFFFFFFFFFFFFFFFFFFFFFF'	
00001370	FFFFFFFF FFFFFFFF					
				772		
				773 *		
				774 * VSTBR	- VECTOR STORE BYTE REVERSED ELEMENTS	
				775 *		
00001378				776	VRX VSTBR, 1	
00001378		00001378		777+	DS OFD	
00001378	00001390			778+	USING *, R5	base for test data and test routine
0000137C	000F			779+T15	DC A(X15)	address of test routine
0000137E	00			780+	DC H' 15'	test number
0000137F	01			781+	DC X' 00'	
00001380	E5E2E3C2 D9404040			782+	DC X' 1'	MB
00001388	00000010			783+	DC CL8' VSTBR'	instruction name
0000138C	00001398			784+	DC A(16)	result length
				785+REA15	DC A(RE15)	result address
				786+*		
00001390				787+	DS OF	
00001390	E610 8E84 100E		00001084	788+X15	VSTBR V1, V10UTPUT, 1	test instruction
00001396	07FB			789+	BR R11	return
00001398				790+RE15	DC OF	xl16 result
00001398				791+	DROP R5	
00001398	01000302 05040706			792	DC XL16' 01000302050407060908111013121514'	
000013A0	09081110 13121514					
				793		
000013A8				794	VRX VSTBR, 2	
000013A8		000013A8		795+	DS OFD	
000013A8	000013C0			796+	USING *, R5	base for test data and test routine
000013AC	0010			797+T16	DC A(X16)	address of test routine
000013AE	00			798+	DC H' 16'	test number
000013AF	02			799+	DC X' 00'	
000013B0	E5E2E3C2 D9404040			800+	DC X' 2'	MB
000013B8	00000010			801+	DC CL8' VSTBR'	instruction name
000013BC	000013C8			802+	DC A(16)	result length
				803+REA16	DC A(RE16)	result address
				804+*		
000013C0				805+	DS OF	
000013C0	E610 8E84 200E		00001084	806+X16	VSTBR V1, V10UTPUT, 2	test instruction
000013C6	07FB			807+	BR R11	return
000013C8				808+RE16	DC OF	xl16 result
000013C8				809+	DROP R5	
000013C8	03020100 07060504			810	DC XL16' 03020100070605041110090815141312'	
000013D0	11100908 15141312					
				811		
000013D8				812	VRX VSTBR, 3	
000013D8		000013D8		813+	DS OFD	
000013D8	000013F0			814+	USING *, R5	base for test data and test routine
000013DC	0011			815+T17	DC A(X17)	address of test routine
000013DE	00			816+	DC H' 17'	test number
				817+	DC X' 00'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000013DF	03			818+	DC	X' 3'	MB
000013E0	E5E2E3C2 D9404040			819+	DC	CL8' VSTBR'	instruction name
000013E8	00000010			820+	DC	A(16)	result length
000013EC	000013F8			821+REA17	DC	A(RE17)	result address
				822+*			
000013F0				823+	DS	0F	
000013F0	E610 8E84 300E		00001084	824+X17	VSTBR	V1, V10OUTPUT, 3	test instruction
000013F6	07FB			825+	BR	R11	return
000013F8				826+RE17	DC	0F	xl16 result
000013F8				827+	DROP	R5	
000013F8	07060504 03020100			828	DC	XL16' 07060504030201001514131211100908'	
00001400	15141312 11100908						
				829			
				830	VRX	VSTBR, 4	
00001408				831+	DS	0FD	
00001408		00001408		832+	USING	*, R5	base for test data and test routine
00001408	00001420			833+T18	DC	A(X18)	address of test routine
0000140C	0012			834+	DC	H' 18'	test number
0000140E	00			835+	DC	X' 00'	
0000140F	04			836+	DC	X' 4'	MB
00001410	E5E2E3C2 D9404040			837+	DC	CL8' VSTBR'	instruction name
00001418	00000010			838+	DC	A(16)	result length
0000141C	00001428			839+REA18	DC	A(RE18)	result address
				840+*			
00001420				841+	DS	0F	
00001420	E610 8E84 400E		00001084	842+X18	VSTBR	V1, V10OUTPUT, 4	test instruction
00001426	07FB			843+	BR	R11	return
00001428				844+RE18	DC	0F	xl16 result
00001428				845+	DROP	R5	
00001428	15141312 11100908			846	DC	XL16' 15141312111009080706050403020100'	
00001430	07060504 03020100						
				847			
				848 *			
				849 * VSTER		- VECTOR STORE ELEMENTS REVERSED	
				850 *			
				851	VRX	VSTER, 1	
00001438				852+	DS	0FD	
00001438		00001438		853+	USING	*, R5	base for test data and test routine
00001438	00001450			854+T19	DC	A(X19)	address of test routine
0000143C	0013			855+	DC	H' 19'	test number
0000143E	00			856+	DC	X' 00'	
0000143F	01			857+	DC	X' 1'	MB
00001440	E5E2E3C5 D9404040			858+	DC	CL8' VSTER'	instruction name
00001448	00000010			859+	DC	A(16)	result length
0000144C	00001458			860+REA19	DC	A(RE19)	result address
				861+*			
00001450				862+	DS	0F	
00001450	E610 8E84 100F		00001084	863+X19	VSTER	V1, V10OUTPUT, 1	test instruction
00001456	07FB			864+	BR	R11	return
00001458				865+RE19	DC	0F	xl16 result
00001458				866+	DROP	R5	
00001458	14151213 10110809			867	DC	XL16' 14151213101108090607040502030001'	
00001460	06070405 02030001						
				868			
				869	VRX	VSTER, 2	
00001468				870+	DS	0FD	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001468		00001468		871+	USING *,R5	base for test data and test routine
00001468	00001480			872+T20	DC A(X20)	address of test routine
0000146C	0014			873+	DC H' 20'	test number
0000146E	00			874+	DC X' 00'	
0000146F	02			875+	DC X' 2'	MB
00001470	E5E2E3C5 D9404040			876+	DC CL8' VSTER'	instruction name
00001478	00000010			877+	DC A(16)	result length
0000147C	00001488			878+REA20	DC A(RE20)	result address
				879+*		
00001480				880+	DS 0F	
00001480	E610 8E84 200F		00001084	881+X20	VSTER V1, V10OUTPUT, 2	test instruction
00001486	07FB			882+	BR R11	return
00001488				883+RE20	DC 0F	xl 16 result
00001488				884+	DROP R5	
00001488	12131415 08091011			885	DC XL16' 12131415080910110405060700010203'	
00001490	04050607 00010203					
				886		
00001498				887	VRX VSTER, 3	
00001498		00001498		888+	DS 0FD	
00001498	000014B0			889+	USING *,R5	base for test data and test routine
0000149C	0015			890+T21	DC A(X21)	address of test routine
0000149E	00			891+	DC H' 21'	test number
0000149F	03			892+	DC X' 00'	
000014A0	E5E2E3C5 D9404040			893+	DC X' 3'	MB
000014A8	00000010			894+	DC CL8' VSTER'	instruction name
000014AC	000014B8			895+	DC A(16)	result length
				896+REA21	DC A(RE21)	result address
				897+*		
000014B0				898+	DS 0F	
000014B0	E610 8E84 300F		00001084	899+X21	VSTER V1, V10OUTPUT, 3	test instruction
000014B6	07FB			900+	BR R11	return
000014B8				901+RE21	DC 0F	xl 16 result
000014B8				902+	DROP R5	
000014B8	08091011 12131415			903	DC XL16' 08091011121314150001020304050607'	
000014C0	00010203 04050607					
				904		
000014C8	00000000			905	DC F' 0'	END OF TABLE
000014CC	00000000			906	DC F' 0'	
				907 *		
				908 *	table of pointers to individual load test	
				909 *		
000014D0				910 E6TESTS	DS 0F	
				911	PTTABLE	
000014D0				912+TTABLE	DS 0F	
000014D0	000010D8			913+	DC A(T1)	TEST &CUR
000014D4	00001108			914+	DC A(T2)	TEST &CUR
000014D8	00001138			915+	DC A(T3)	TEST &CUR
000014DC	00001168			916+	DC A(T4)	TEST &CUR
000014E0	00001198			917+	DC A(T5)	TEST &CUR
000014E4	000011C8			918+	DC A(T6)	TEST &CUR
000014E8	000011F8			919+	DC A(T7)	TEST &CUR
000014EC	00001228			920+	DC A(T8)	TEST &CUR
000014F0	00001258			921+	DC A(T9)	TEST &CUR
000014F4	00001288			922+	DC A(T10)	TEST &CUR
000014F8	000012B8			923+	DC A(T11)	TEST &CUR
000014FC	000012E8			924+	DC A(T12)	TEST &CUR

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001500	00001318			925+	DC	A(T13)	TEST &CUR
00001504	00001348			926+	DC	A(T14)	TEST &CUR
00001508	00001378			927+	DC	A(T15)	TEST &CUR
0000150C	000013A8			928+	DC	A(T16)	TEST &CUR
00001510	000013D8			929+	DC	A(T17)	TEST &CUR
00001514	00001408			930+	DC	A(T18)	TEST &CUR
00001518	00001438			931+	DC	A(T19)	TEST &CUR
0000151C	00001468			932+	DC	A(T20)	TEST &CUR
00001520	00001498			933+	DC	A(T21)	TEST &CUR
				934+*			
00001524	00000000			935+	DC	A(0)	END OF TABLE
00001528	00000000			936+	DC	A(0)	
				937			
0000152C	00000000			938	DC	F' 0'	END OF TABLE
00001530	00000000			939	DC	F' 0'	

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT	
					941	*****
					942	* Register equates
					943	*****
			00000000	00000001	945 R0	EQU 0
			00000001	00000001	946 R1	EQU 1
			00000002	00000001	947 R2	EQU 2
			00000003	00000001	948 R3	EQU 3
			00000004	00000001	949 R4	EQU 4
			00000005	00000001	950 R5	EQU 5
			00000006	00000001	951 R6	EQU 6
			00000007	00000001	952 R7	EQU 7
			00000008	00000001	953 R8	EQU 8
			00000009	00000001	954 R9	EQU 9
			0000000A	00000001	955 R10	EQU 10
			0000000B	00000001	956 R11	EQU 11
			0000000C	00000001	957 R12	EQU 12
			0000000D	00000001	958 R13	EQU 13
			0000000E	00000001	959 R14	EQU 14
			0000000F	00000001	960 R15	EQU 15
					962	*****
					963	* Register equates
					964	*****
			00000000	00000001	966 V0	EQU 0
			00000001	00000001	967 V1	EQU 1
			00000002	00000001	968 V2	EQU 2
			00000003	00000001	969 V3	EQU 3
			00000004	00000001	970 V4	EQU 4
			00000005	00000001	971 V5	EQU 5
			00000006	00000001	972 V6	EQU 6
			00000007	00000001	973 V7	EQU 7
			00000008	00000001	974 V8	EQU 8
			00000009	00000001	975 V9	EQU 9
			0000000A	00000001	976 V10	EQU 10
			0000000B	00000001	977 V11	EQU 11
			0000000C	00000001	978 V12	EQU 12
			0000000D	00000001	979 V13	EQU 13
			0000000E	00000001	980 V14	EQU 14
			0000000F	00000001	981 V15	EQU 15
			00000010	00000001	982 V16	EQU 16
			00000011	00000001	983 V17	EQU 17
			00000012	00000001	984 V18	EQU 18
			00000013	00000001	985 V19	EQU 19
			00000014	00000001	986 V20	EQU 20
			00000015	00000001	987 V21	EQU 21







SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
R8	U	00000008	1	953	156	160	161	162	164	
R9	U	00000009	1	954	157	164	165	167		
RE1	F	000010F8	4	528	523					
RE10	F	000012A8	4	693	688					
RE11	F	000012D8	4	715	710					
RE12	F	00001308	4	733	728					
RE13	F	00001338	4	751	746					
RE14	F	00001368	4	769	764					
RE15	F	00001398	4	790	785					
RE16	F	000013C8	4	808	803					
RE17	F	000013F8	4	826	821					
RE18	F	00001428	4	844	839					
RE19	F	00001458	4	865	860					
RE2	F	00001128	4	546	541					
RE20	F	00001488	4	883	878					
RE21	F	000014B8	4	901	896					
RE3	F	00001158	4	564	559					
RE4	F	00001188	4	582	577					
RE5	F	000011B8	4	600	595					
RE6	F	000011E8	4	618	613					
RE7	F	00001218	4	636	631					
RE8	F	00001248	4	654	649					
RE9	F	00001278	4	675	670					
REA1	A	000010EC	4	523						
REA10	A	0000129C	4	688						
REA11	A	000012CC	4	710						
REA12	A	000012FC	4	728						
REA13	A	0000132C	4	746						
REA14	A	0000135C	4	764						
REA15	A	0000138C	4	785						
REA16	A	000013BC	4	803						
REA17	A	000013EC	4	821						
REA18	A	0000141C	4	839						
REA19	A	0000144C	4	860						
REA2	A	0000111C	4	541						
REA20	A	0000147C	4	878						
REA21	A	000014AC	4	896						
REA3	A	0000114C	4	559						
REA4	A	0000117C	4	577						
REA5	A	000011AC	4	595						
REA6	A	000011DC	4	613						
REA7	A	0000120C	4	631						
REA8	A	0000123C	4	649						
REA9	A	0000126C	4	670						
READDR	A	00000014	4	430	229					
REG2LOW	U	000000DD	1	377						
REG2PATT	U	AABBCCDD	1	376						
RELEN	A	00000010	4	429						
RPTDWSAV	D	000003B0	8	302	289	293				
RPTERROR	I	00000342	4	269	242					
RPTSAVE	F	000003A4	4	299	269	296				
RPTSVR5	F	000003A8	4	300	270	295				
SKL0001	U	0000005D	1	186	202					
SKT0001	C	0000022A	26	183	186	203				
SVOLDPSW	U	00000140	0	121						
T1	A	000010D8	4	517	913					







DESC	SYMBOL	SIZE	POS	ADDR
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**Entry: 0**

Image	IMAGE	5428	0000- 1533	0000- 1533
Regi on		5428	0000- 1533	0000- 1533
CSECT	ZVE6TST	5428	0000- 1533	0000- 1533

STMT	FILE NAME
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100	100

```
1 /home/tn529/sharedvfp/tests/zvector-e6-02-stores.asm
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**\*\* NO ERRORS FOUND \*\***